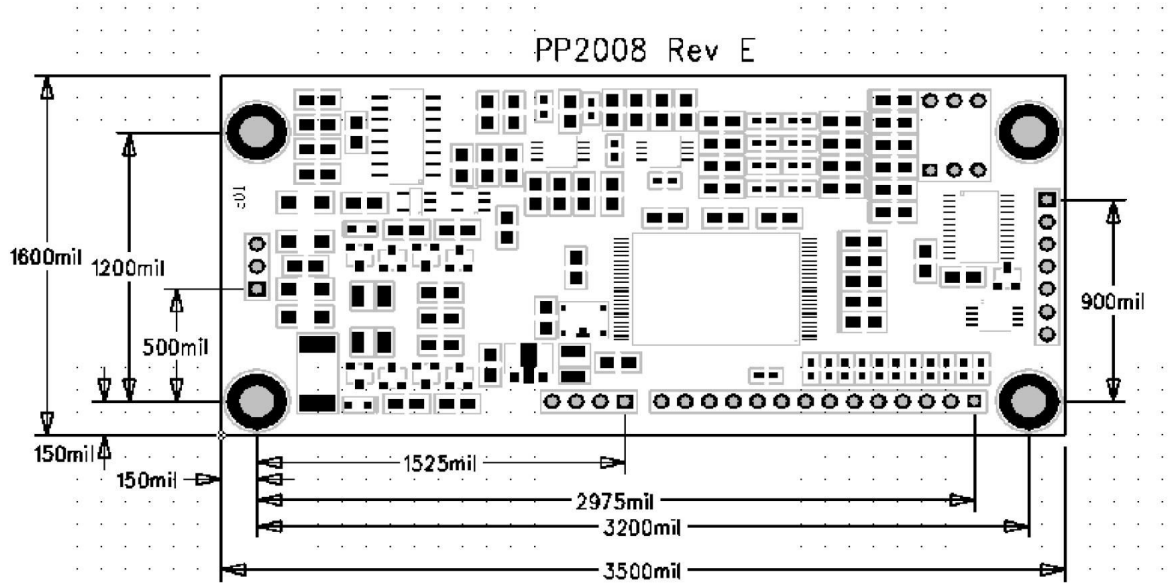
PP2008 外形寸法


PP2008 Rev E
1600mil
1200mil
500mil
150mil
150mil
1525mil
2975mil
3200mil
3500mil
900mil

7.6 Signal Pin Definitions

The pin definitions are as shown below.

Connector	Function	Pin	Description
J1	Host Port	1	Network or Transparent Mode Selection
		2	External Hardware Reset
		3	RS232 Receive Data - PP2008 output (Host - UARTA)
		4	RS232 Clear To Send - PP2008 output (Host - UARTA)
		5	RS232 Transmit Data – PP2008 input (Host - UARTA)
		6	RS232 Request To Send – PP2008 input (Host - UARTA)
		7	Ground (Host)
J2	Power	1	VCC +5 vdc power
		2	VEE -5 vdc power
		3	Power Ground
		4	Analog +5 vdc (for A/D)
J3	Carrier	1	Modulated carrier
		2	Modulated carrier
		3	Drive Enable (equivalent to DRVEN from ICSS1003, pin 23)
J4	SPI bus and field I/O	1	SPI Bus SO (output)
		2	SPI Bus CLK (clock)
		3	SPI Bus SI (input)
		4	SPI Bus external Chip Select (equivalent to ICSS1002 pin 26)
		5	Discrete I/O bit 0
		6	Discrete I/O bit 1
		7	Discrete I/O bit 2
		8	Discrete I/O bit 3
		9	Discrete I/O bit 4
		10	Discrete I/O bit 5
		11	Discrete I/O bit 6
		12	Discrete I/O bit 7
		13	Analog Input sense
		14	Analog input ground
J5	Programming Port	1	RS232 PP2008 output (UART B)
		2	RS232 PP2008 input (UART B)
		3	Ground

The functions and operation of J1, J2, and J3 are similar to the PowerPlex1000, with additional pins added. J4 supports the SPI bus and discrete and analog I/O, and J5 supports in-circuit emulation. Refer to the COP data sheet for the electrical characteristics of the field I/O pins, which are connected directly to the processor.

7.7 Environmental Specifications

PP2008 shall operate within the industrial temperature, range,

PP2008 shall be designed for ROHS conformance.

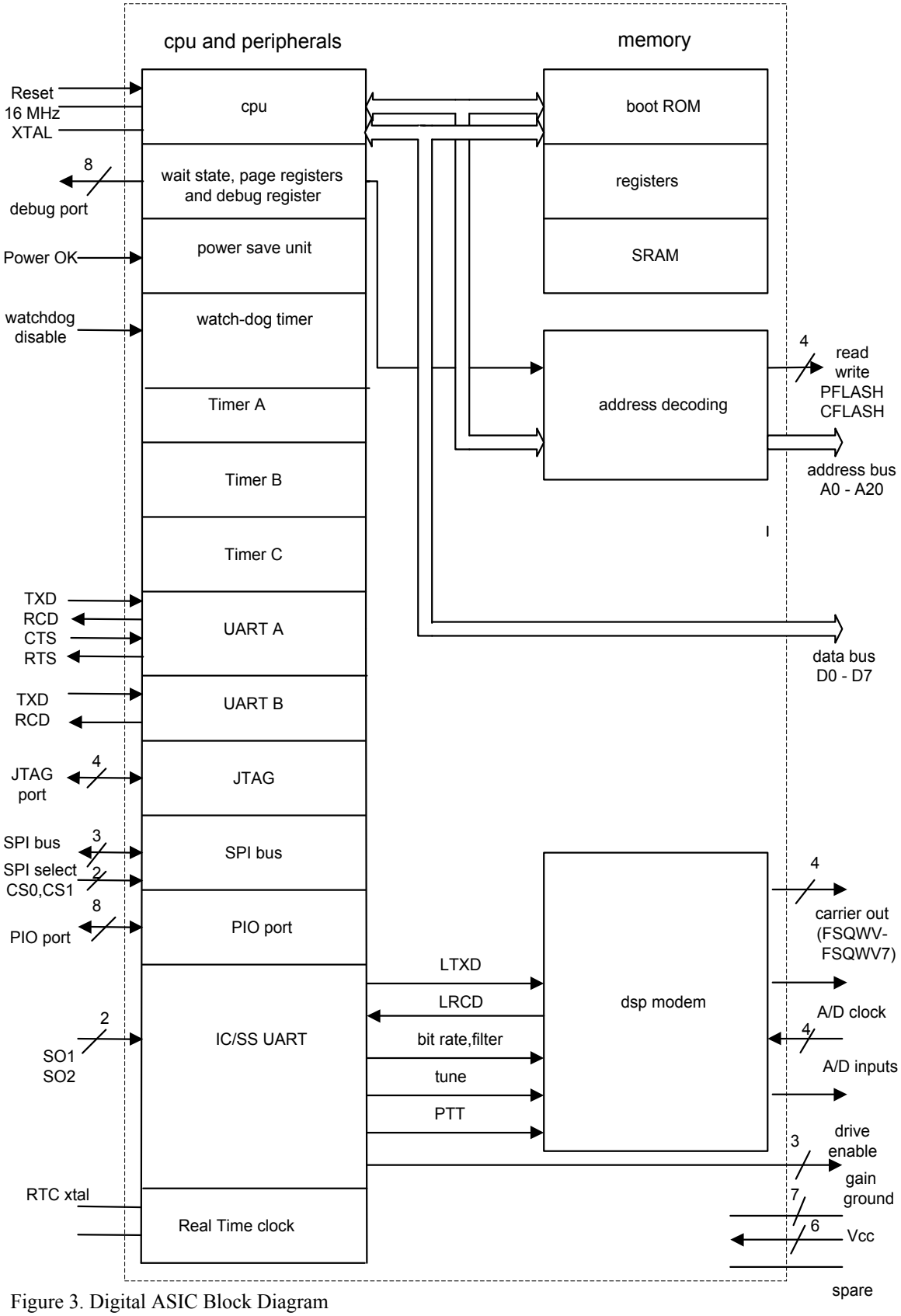


Figure 3. Digital ASIC Block Diagram